AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes a change to Fig. 3B to change the notation from 2/3A to --2A/3--.

Attachment: Replacement Sheet containing Figs. 3A and 3B

REMARKS

In the Office Action, the Examiner required a new Title; objected to claim 6; and rejected claims 1-11 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,716,046 of Mistry ("Mistry") and U.S. Patent No. 5,918,134 of Gardner et al. ("Gardner").

Applicant has amended the Title. Applicant has also amended claims 1 and 6 and canceled claims 2, 3, 8, and 9. Further, Applicant has amended Fig. 3B. Claims 1, 4-7, and 10-19 remain pending, with claims 12-19 withdrawn from consideration.

In response to the Examiner's requirement for a new Title, Applicant has amended the Title to be more clearly indicative of the invention to which the claims are directed.

The Examiner objected to claim 6 because the limitation "the recess" does not have sufficient antecedent basis. In response, Applicant has amended claim 6 to recite "a recess," which overcomes the Examiner's ground for objection. Applicant therefore requests that the Examiner withdraw his objection to claim 6.

Applicant has amended Fig. 3B to correct an inadvertent error therein. In particular, the dimension "2/3A" has been corrected to --2A/3--. Applicant's specification supports this correction at, for example, page 19, lines 2-5. Applicant attaches herewith a replacement drawing sheet containing Fig. 3A and amended Fig. 3B.

Applicant respectfully traverses the Examiner's rejection of claims 1-11 as unpatentable over Mistry and Gardner. Initially, Applicant notes that this rejection has been rendered moot against claims 2, 3, 8, and 9 by the cancellation of those claims.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or

suggest all the claim elements. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. *See* M.P.E.P. § 2143.

In his rejection, the Examiner cites features shown in Fig. 2 of Mistry. Mistry, in Fig. 2, discloses a MOSFET 200 including a gate dielectric 211 that conforms to a recess in a wafer 102.

> The recess has a bottom portion [sic] and substantial vertical sidewalls. . . . source/drain extensions 205 are disposed adjacent gate dielectric 211, and deep source/drain regions 204 are disposed substantially [sic] wafer 102. . . . by providing transistor 200 with a recessed channel region, source/drain extension 205 may be elevated with respect thereto.

Mistry at column 5, lines 27-41.

The Examiner admits that "Mistry does not explicitly show that the depth of the recess is no more than 6 nm," as required by Applicant's independent claims 1 and 6. (Office Action at page 3.) Mistry also fails to disclose either in Fig. 2 or the description thereof whether each extension 205 includes an extended portion that extends under the gate electrode.

The Examiner alleges that Gardner teaches that "it is preferable to make gate insulating films 132 between 3 and 30 nm" (Office Action at Page 3). At column 5, lines 63 et seq., Gardner describes "the formation of spacer structures 125 having an outer surface 124." According to Fig. 5, these structures include spacer structures 125a and 125b. Gardner further describes at column 6, lines 17 et seq., with reference to Fig. 6, that "a channel dielectric 126 is formed between first and second spacer structures 125a and 125b." Gardner further describes at col. 6, lines 24 et seq., with reference to

Fig. 7, that "outer surface 124 of spacer structure 125 is removed and a first species 128 is introduced into peripheral region 105 of channel region 106. . . . The presence of channel dielectric 126 prevents first species 128 from occurring in the interior region 109 of channel 106." At column 6, lines 49 et seq., Gardner describes with reference to Fig. 8, that "channel dielectric 126 and spacer structure 120 have been removed and a gate dielectric structure 132 has been formed on an upper surface of channel region 106. Gate dielectric 132 is preferably comprised of a thermal oxide having a thickness of 30-300 angstroms." Thus, Gardner describes gate dielectric structure 132 as having a thickness of 30-300 angstroms. However, gate dielectric structure 132 is formed on the entire upper surface of channel region 106 and the thickness of gate dielectric structure 132 does not define the depth of a recess that appears to result from the prior formation of channel dielectric 126. Instead, the depth of the apparent recess, which does not appear to be described in the specification of Gardner, appears to be related to the thickness of channel dielectric 126. However, Gardner does not disclose the thickness of channel dielectric 126. Therefore, Gardner does not disclose the depth of any recess that may be present in Fig. 8.

Further, Gardner does not disclose any features relating to extension regions of a source region and a drain region.

The Examiner has failed to establish a *prima facie* case of obviousness because, at the very least, the applied references do not teach or suggest all of the claim elements of either of independent claims 1 and 6. Specifically, Mistry and Gardner taken separately or in combination, fail to disclose or suggest a semiconductor device recited in Applicant's claim 1 comprising a combination including "a semiconductor

substrate having a recess whose depth is not more than 6 nm; . . . wherein a depth of the recess from a surface of the semiconductor substrate is deeper than a depth from the surface of the semiconductor substrate of an impurity concentration peak in [an] extension region, and wherein the extension regions are opposite to each other, each extension region including an extended portion that extends under [a] gate electrode, and a length of the extended portion is less than two-thirds of a depth from the surface of the semiconductor substrate in the extension region." Applicant's independent claim 6 recites similar features also not disclosed or suggested by Mistry and Gardner taken separately or in combination.

Since the Examiner fails to establish a *prima facie* case of obviousness, Applicant submits that the Section 103(a) rejection of independent claims 1 and 6 should be withdrawn. In addition to claims 1 and 6, Applicant further submits that claims 4, 5, 7, 10, and 11 are also patentable at least due to their dependence from one of claims 1 and 6.

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: May 23, 2005

By: _____
Richard V. Burgujian
Reg. No. 31,744

Attachment: Replacement Sheet containing Figs. 3A and 3B